

## ESR, Stability, and the LDO Regulator

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### ABSTRACT

Choosing an output capacitor for LDO regulators with PNP or PMOS pass element can be difficult due to specific ESR requirements. This application note explains why higher ESR capacitors are necessary, how to choose them, and how to determine whether or not the regulator is stable.

As shown in the typical PMOS or PNP open loop gain plot of Figure 1, there are three important poles in a PMOS or PNP pass element based LDO regulator. The dominant pole,  $P_{(DOM)}$ , is set in the regulator's error amplifier. The load pole,  $P_{(LOAD)}$ , is formed by the output capacitor and load and therefore varies with load current. The pass device pole,  $P_{(PASS)}$ , is formed by the parasitic capacitance of the pass element. In order for any negative feedback system to be stable, the open loop gain of the system must be below 0 dB when the phase is  $360^\circ$  ( $180^\circ$  of the fed-back signal plus the  $180^\circ$  from the inverting input of the error amplifier).

Stated another way, the system must have sufficient phase margin, i.e., the amount of phase shift remaining until  $360^\circ$  degree when the gain is at 0 dB. Since each pole contributes  $90^\circ$  of phase shift and 20dB/decade (or  $-1$ ) rolloff in gain, a three-pole, high gain system requires compensation in order to be stable. A regulator is unconditionally stable (i.e., has sufficient phase margin) if the open loop gain curve rolls off at 20dB/decade (i.e., like a single pole system) before crosses 0 dB. The most common method of compensation is to insert a zero in the system to cancel the phase shift and rolloff of one of the poles. Since an LDO already requires an output capacitor for normal operation, using the output capacitor's ESR is typically the simplest and least expensive method for generating this zero.

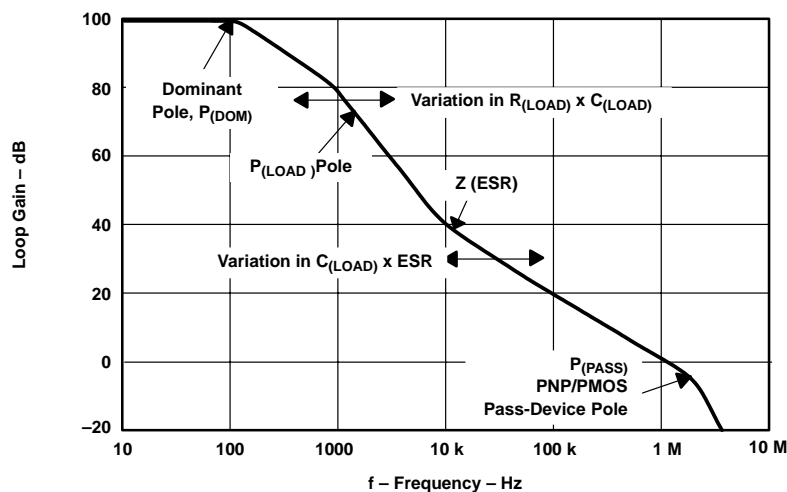
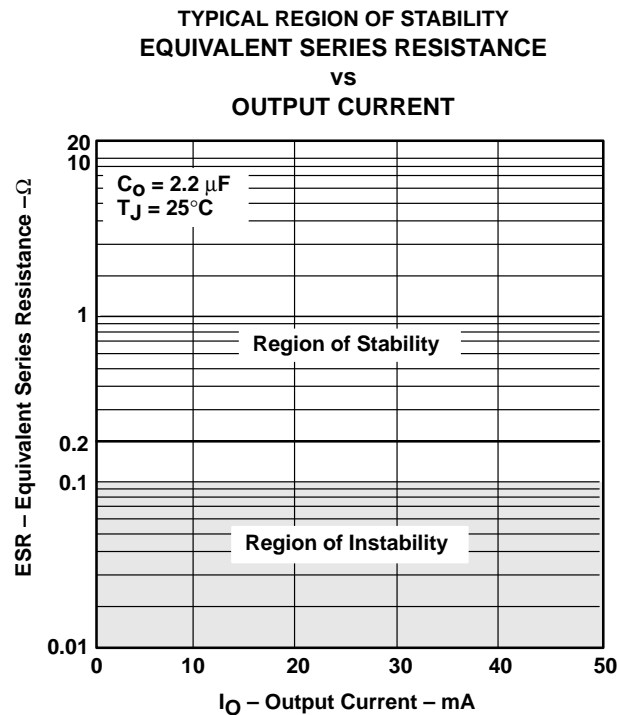


Figure 1. Open Loop Response of Typical PMOS or PNP LDO Regulator

The challenge is choosing a capacitor with the correct amount of ESR. The ESR must be high enough to lower the  $Z_{(ESR)}$  frequency so that the gain slope is  $-20$  dB/decade instead of  $-40$  dB/decade ( $-2$ ) when it crosses  $0$  dB, but low enough so that the  $Z_{(ESR)}$  frequency is high enough for the gain to be below  $0$  dB before  $P_{(PASS)}$ .

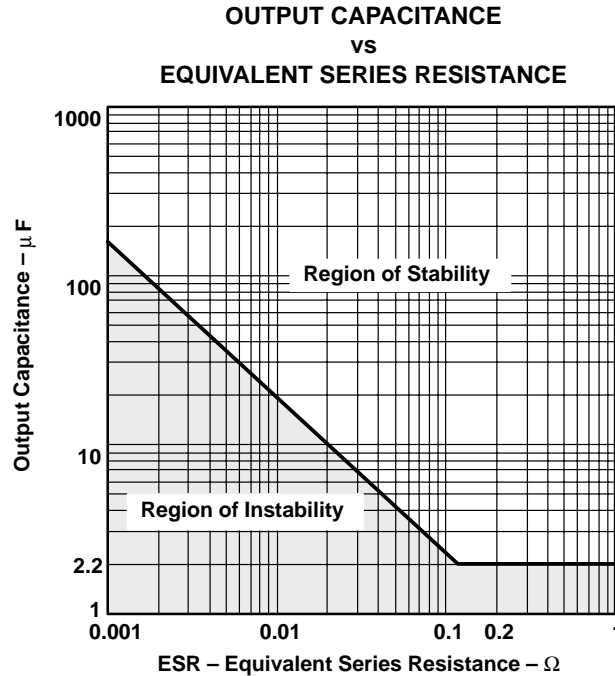
In most of TI's regulator data sheets, a minimum capacitor value is specified and an ESR vs output current for that output capacitor (and usually another capacitor) is provided. A typical curve for the TPS76050 is shown in Figure 2.



This device's curve requires that, for the minimum  $2.2\text{-}\mu\text{F}$  output capacitor, the ESR must be between  $0.1\ \Omega$  and  $20\ \Omega$ . Few capacitors have more than  $2\ \Omega$  of ESR, so the upper limit on the ESR can usually be ignored. The lower limit actually sets the maximum value for the  $Z_{(ESR)}$ . For the case of  $2.2\text{-}\mu\text{F}$  capacitor referenced in Figure 2, the maximum value for:

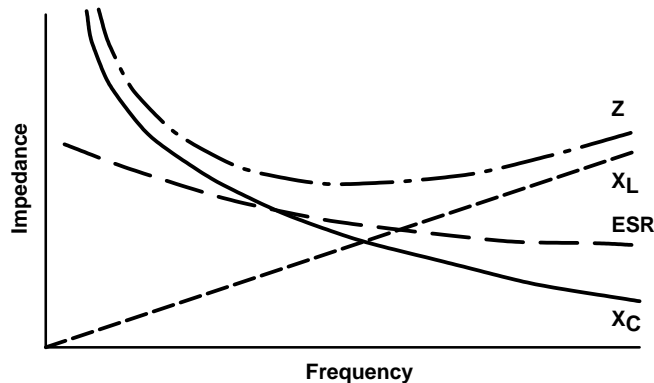
$$Z_{(ESR)} = 1/(2 \times \pi \times R_{(ESR)} \times C_O) = 72.3\ \text{kHz}$$

Thus any capacitance and ESR product larger than  $0.1 \times 2.2 \times 10^{-6} = 2.2 \times 10^{-7}$  (but less than  $20 \times 2.2 \times 10^{-6} = 4.4 \times 10^{-5}$ ) is stable, as long as the capacitance is above the minimum required capacitance value. A curve demonstrating this is shown in Figure 3. LDO regulators using larger capacitors are stable with smaller ESRs. In fact, larger capacitance and/or smaller ESR values improve output transient responses.



**Figure 3. Example Output Capacitance vs ESR**

Figure 4 shows the general shape of an impedance curve for a capacitor. A capacitor begins capacitive ( $X_C$ ) then becomes resistive (ESR) near its resonance point and finally becomes inductive ( $X_L$ ) at high frequencies. The impedance curve ( $Z$ ) is the combination of each of these components.

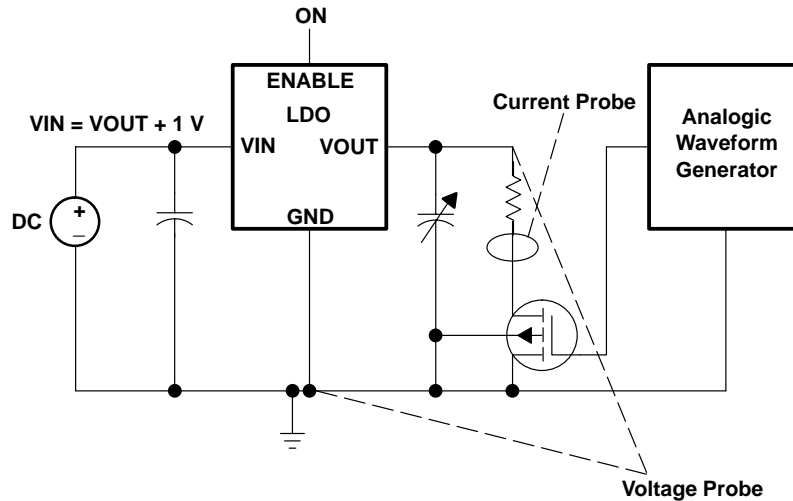


**Figure 4. General Shape of an Impedance Curve for a Capacitor**

Capacitors are usually rated with a maximum ESR at a certain frequency. This frequency is typically between 10 kHz and 100 kHz and is near the resonance point. To be certain that the capacitor's minimum ESR does not go below the minimum ESR requirement, the designer should request ESR vs frequency curves over the entire temperature range of interest from the manufacturer. Some manufacturers may supply this information. If only impedance curves are available, the region where the curve stops sloping downward and flattens out is where the capacitor's ESR dominates over the capacitance.

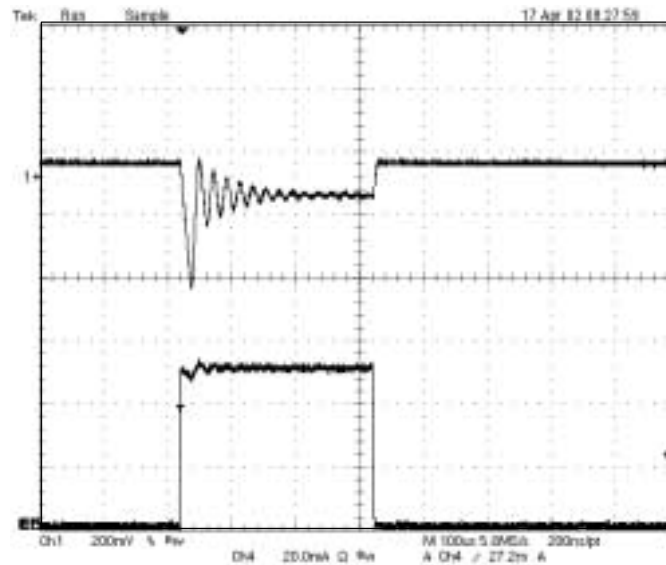
It is also acceptable to place a small, low ESR, resistor in series with a ceramic capacitor. The resistor must have a tolerance over temperature that keeps its value within the limits of the stability curves.

Performing a load transient test and observing the amount of ringing on the output is the best way to determine if the capacitor selected is stable. Figure 5 shows a test setup for a load transient test using a MOSFET switch and function generator. This setup is preferable to most electronic loads because the simulated transient is much faster.



**Figure 5. Load Transient Setup**

Figure 6 shows the measured results using a TPS76050 device with a 2.2- $\mu\text{F}$  ceramic (low ESR) capacitor. Figure 7 shows the measured results of a TPS76050 device with a 2.2- $\mu\text{F}$  and a 1- $\Omega$  series resistor. The results in Figure 6 show multiple oscillations or rings after the initial spike, indicating instability, while the results in Figure 7 show a stable load transient. Typically, four rings or less indicate sufficient phase margin for the device to be stable.



**Figure 6. TPS76050 Load Transient With 2.2- $\mu\text{F}$  Ceramic Capacitor**

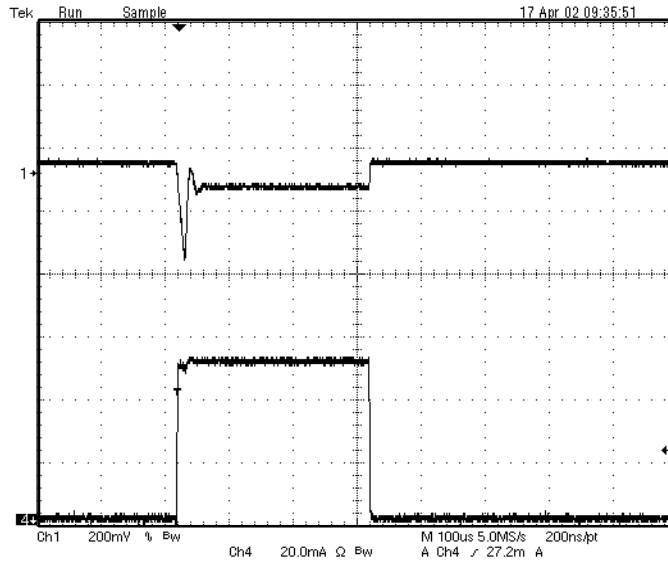


Figure 7. TPS76050 Load Transient With 2.2- $\mu$ F Ceramic Capacitor and 1- $\Omega$  ESR

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